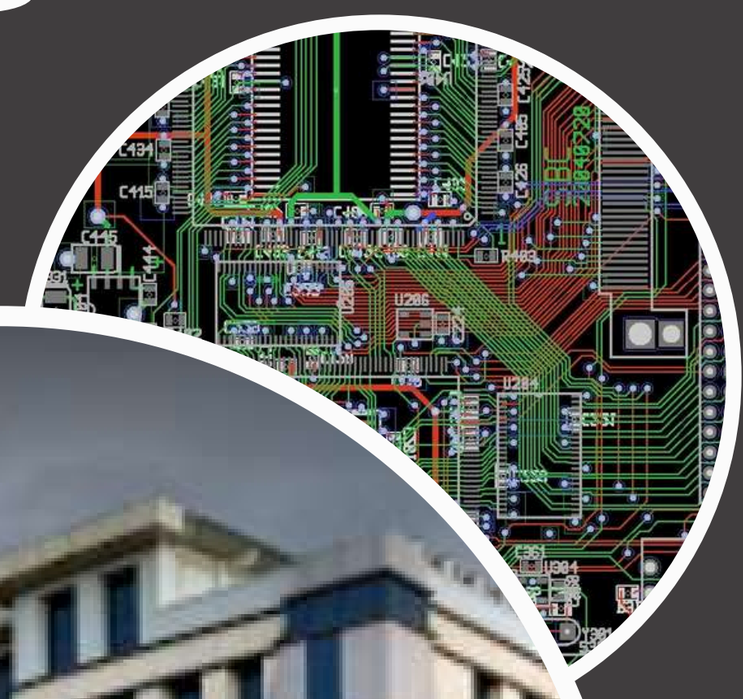
IIIT Guwahati & TTTC INDIA Presents

VLSI TEST WORKSHOP

7th to 9th March 2025

09:00 AM to 06:00 PM

IIIT Guwahati



Key Features

- Design for Testing
- Fault Modeling
- Test Generation
- Test Standards
- Test Diagnosis
- Scan Compression and Logic BIST
- Memory Testing

Perks

- Learn from Industry Leaders
- Networking opportunities
- Hands-on Lab Session on VLSI Testing
- Career Guidance
- Internship/Placement Opportunities

Coordinator : Dr. Rakesh Biswas

b.rakesh@iiitg.ac.in

PATRON

Prof. Sarat Kumar Patra
Director
IIIT GUWAHATI

ADVISORY COMMITTEE

Dr. Mourina Ghosh
Head of the Department
ECE, IIIT GUWAHATI

Dr. Subhasish Dhal
Head of the Department
CSE, IIIT GUWAHATI

COORDINATOR

Dr. Rakesh Biswas

Co-COORDINATOR

Dr. Sheikh Wasmir Hussain

REGISTRATION

IIITG Students	**FREE**
Students other than IIITG	**Rs 850/- ***
Faculties other than IIITG	**Rs 1500/- ***
Industry Professionals	**Rs 2000/- ***

* Includes Registration Kit, Refreshment & Lunch
- Participation Certificate
- Limited seats based on First Come First Serve basis
- Accommodation in student hostels to limited participants, subject to availability, on a paid basis.

RESOURCE PERSONS

INDRANIL SENGUPTA
Professor
Department of Computer Science,
IIT Kharagpur

ABHISHEK CHAUDHARY
Principal Member of Technical Staff,
AMD

JYOTIRMOY SAIKIA
Software Architect,
Cadence

RAJIT KARMAKAR
Member of Technical Staff,
Silicon Design Engineering,
AMD

For more details, please contact
Dr. Rakesh Biswas
Dr. Sheikh Wasmir Hussain

VLSI TEST WORKSHOP

EVENT SCHEDULE

7th March, 2025, FRIDAY

Day 1

09:00AM - 09:30AM Inauguration and Introduction
09:30AM - 10:30AM Introduction to Design for Test-1
10:30AM - 11:00AM Networking over Tea/Coffee
11:00AM - 12:30PM Introduction to Design for Test-2
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:45PM Fault models
02:45PM - 03:00PM Networking over Tea/Coffee
03:00PM - 04:45PM Fault Simulation and Test Generation
04:45PM - 05:45PM DFT as a career

8th March, 2025, SATURDAY

Day 2

09:00AM - 10:30AM Scan Based Testing
10:30AM - 11.00AM Networking over Tea/Coffee
11.00AM - 12:30PM Scan Compression & Logic BIST
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:30PM Test Diagnosis
02:30PM - 02:45PM Networking over Tea/Coffee
02:45PM - 04:00PM Memory Testing
04.00PM - 05:45PM Test Standards

9th March, 2025, SUNDAY

Day 3

09:00AM - 10:30AM Lab session - 1
10:30AM - 10.45AM Networking over Tea/Coffee
10.30AM - 12:30PM Lab Session – 2
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:00PM Open house and conclusion
02:00PM - 03:30PM Lab session – 3
03:30PM - 03:45PM Networking over Tea/Coffee

IEEE COMPUTER SOCIETY TTTC
Test Technology Technical Community